REMARKS

The foregoing amendment is to impart greater clarity and to broaden the claims rather than to avoid prior art.

Applicants respectfully request reconsideration of this application as amended. Claims 1-29 are pending in the application. Claims 1-16 and 24-29 are rejected. Claims 17-23 are allowed. Claims 1 and 24-29 are amended.

The Office Action rejects Claims 1-16 for nonstatutory obviousness type double patenting over U.S. Patent No. 6,418,529. Applicant respectfully disagrees that all claims indicated in the present application are obvious in view of the instant patented claims. Never the less, a terminal disclaimer is attached herewith as a separate paper.

Rejections under 35 U.S.C. 101

Claims 1-9 and 24-29 are rejected under 35 U.S.C. 101, as allegedly being directed to non-statutory subject matter. Applicant respectfully disagrees.

An analysis of the instant claims must be performed in order to make a determination of whether the subject matter is statutory. Such analysis should correlate each claim element with corresponding structures, materials or acts set forth in the specification.

The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips v. AWH Corp.*, 415 F.3d at 1313.

Claim 1, for example, sets forth:

1. (Currently Amended) A computer implemented method comprising:
responsive to a first single instruction, identifying a first operand including four packed data elements, (r_3, r_2, r_1 and r_0), and identifying a second operand including four packed coefficients, (w_3, w_2, w_1 and w_0), generating four packed first products, (r_3w_3, r_2w_2, r_1w_1 and r_0w_0) and storing said four packed first products at a first destination identified by said first single instruction;
responsive to a second single instruction, identifying a third operand including four packed data elements, (s_3, s_2, s_1 and s_0), and identifying a fourth operand including four packed coefficients, (w_7, w_6, w_5 and w_4), generating four packed second products, (s_3w_7, s_2w_6, s_1w_5 and s_0w_4) and storing said four packed second products at a second destination identified by said second single instruction; and
responsive to a third single instruction, identifying a fifth operand including the four packed first products and identifying a sixth operand including the four packed second products, generating four packed sums, ($s_2w_6+s_3w_7$, $s_0w_4+s_1w_5$, $r_2w_2+r_3w_3$, and $r_0w_0+r_1w_1$) and storing them at a third destination identified by said third single instruction.

With regard to Claims 1-9, the instant claims as amended, set forth a computer implemented method, which would be apparent to a person of skill in the art in the context of the entire patent, including the specification (e.g. Figs. 4a-4l; pars. 53-63) to utilize SIMD multiplication instructions and a horizontal intra-add instruction in performing a butterfly computation as may be employed, for example, in Fast-Fourier Transforms thus having practical applications in the technical arts.

Similarly Claim 14, sets forth:

14. (Currently Amended) An article of manufacture including one or more recordable media having executable instructions stored thereon including a first instruction and a second instruction which, when executed by a processing device, cause the processing device to:
access a first packed data operand, containing at least an A data element and a B data element packed together at a first storage area;
access a second packed data operand containing at least a C data element and a D data element packed together at a second storage area;
add the A data element and the B data element to generate a first result element of a third packed data in response to said first instruction;
add the C data element and the D data element to generate a second result element of the third packed data in response to said first instruction;
access a fourth storage area for storing a fourth packed data operand

containing at least a E data element and a F data element packed together;

access the second packed data operand containing at least the C data element and the D data element packed together at the second storage area;

subtract the E data element and the F data element to generate a third result element of a fifth packed data in response to said second instruction; and

subtract the C data element and the D data element to generate a fourth result element of the fifth packed data in response to said first instruction.

Claims 24, as amended, sets forth an article of manufacture to realize the functionality of executable instructions. The instant language when correlated with the corresponding structures and processes set forth in the specification (e.g. Figs. 3a-3b; pars. 47-52) makes it apparent to one of skill in the art that the claimed invention can utilize horizontal intra-addition/subtraction in performing a butterfly computation as may be employed, for example, in Walsh-Hadamard transforms thus also having practical applications in the technical arts.

Thus Applicant respectfully submits that Claims 1-9 and 24-29, as amended, are directed to statutory subject matter.

CONCLUSION

Applicants respectfully submit the amended specification, and the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 50-0221 for any charges that may be due.

Respectfully submitted,

Date: June 21, 2007

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